

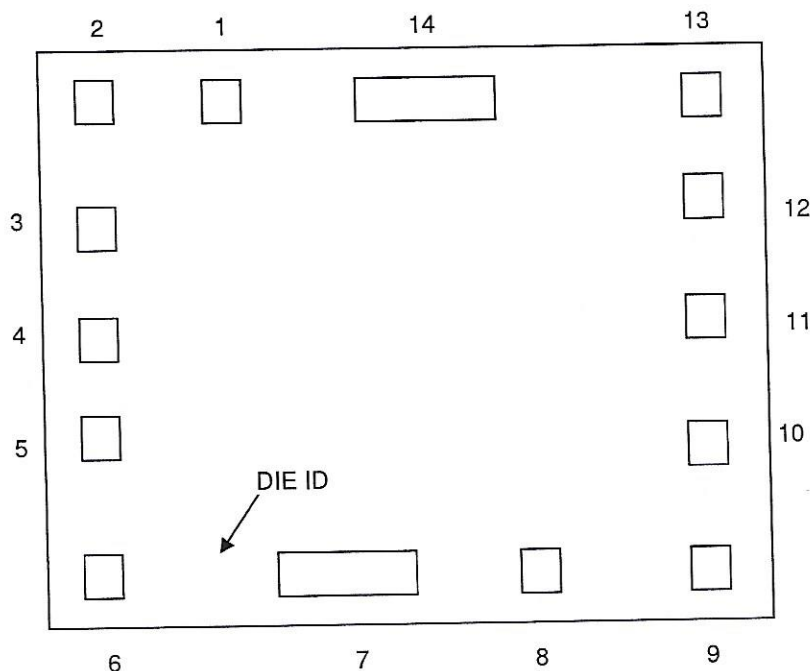


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD	FUNCTION
1	1 $\bar{R}$
2	1D
3	1CP
4	1 $\bar{S}$
5	1Q
6	1 $\bar{Q}$
7	GND
8	2 $\bar{Q}$
9	2Q
10	2 $\bar{S}$
11	2CP
12	2D
13	2 $\bar{R}$
14	V <sub>CC</sub>

**Top Material: Aluminum**  
**Backside Material: Silicon**  
**Bond Pad Size: .004" X .004" min.**  
**Backside Potential: Vcc or Float**  
**Mask Ref: 0234**

**APPROVED BY: DK**

**DIE SIZE .055 x .067"**

**DATE: 9/16/16**

**MFG: Zytrex Semi.**

**THICKNESS .025"**

**P/N: 54HCT74**