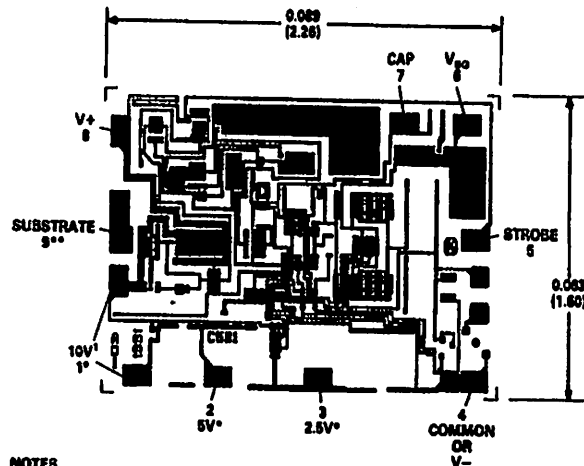


Sierra Components, Inc.

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



NOTES
 *BOTH 10V PADS MUST BE CONNECTED TO THE OUTPUT.
 **INTERCONNECTIONS REQUIRED; SEE PIN DESIGNATIONS FOR INFORMATION.
 **NOT BROUGHT OUT IN PACKAGE DEVICE.
 PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8-PIN METAL PACKAGE.

REV. A

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:
MFG: Analog Devices

DIE SIZE (Mils): 89 X 63
THICKNESS:

DATE: 10/19/98
P/N: AD584

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