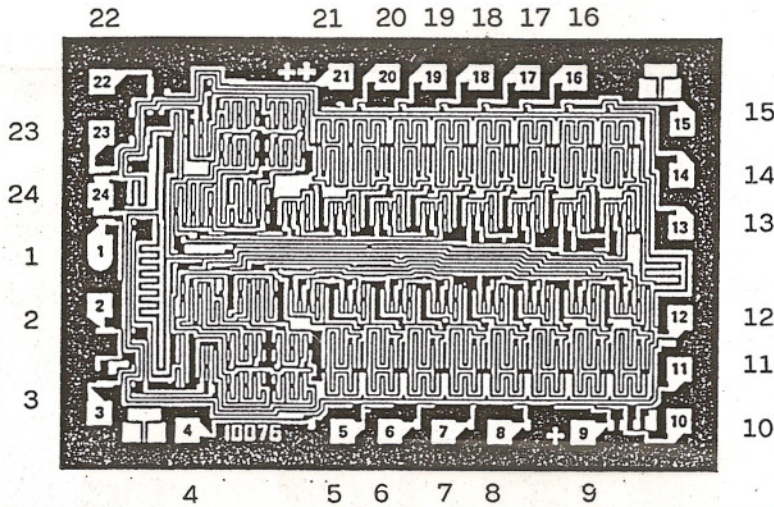




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



<u>Pad</u>	<u>Function</u>	<u>Pad</u>	<u>Function</u>	<u>Pad</u>	<u>Function</u>
1	Strobe	9	S1	17	S9
2	Data 1	10	S2	18	S8
3	Data 2	11	S0	19	S11
4	S7	12	VSS	20	S10
5	S6	13	S13	21	Data 3
6	S5	14	S12	22	Data 4
7	S4	15	S15	23	Inhibit
8	S3	16	S14	24	VDD

Topside Metal: Al
Backside: Si
Backside Potential: VDD
Mask Ref: 10076
Bond Pads (Mils): 4mils sq.

APPROVED BY:
MFG: Harris

DIE SIZE (Mils): 113 x 75
THICKNESS: 20mils

DATE: 3/13/00
P/N: CD4515BH