

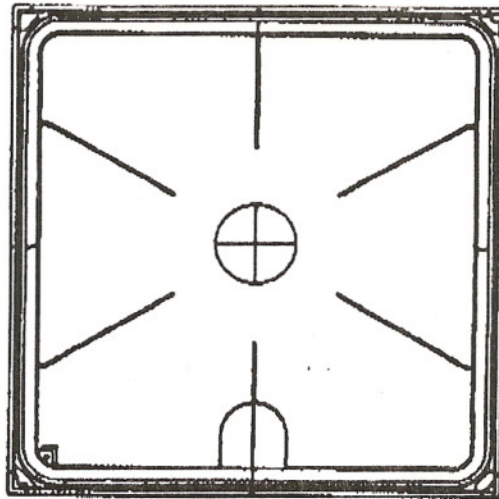


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**DIE SIZE:** 240 x 240 mils

**SOURCE ATTACH AREA** 40 mil Diameter

**GATE ATTACH AREA** 32 x 32 mils

**BACK SIDE DRAIN**

**Topside Metal:** -  
**Backside:** -  
**Backside Potential:** -  
**Mask Ref:** -  
**Bond Pads:** -

**APPROVED BY:** CD

**MFG:** Harris

**DIE SIZE:** .240" x .240"

**THICKNESS:** -

**DATE:** 7/25/02

**P/N:** FRC450R