



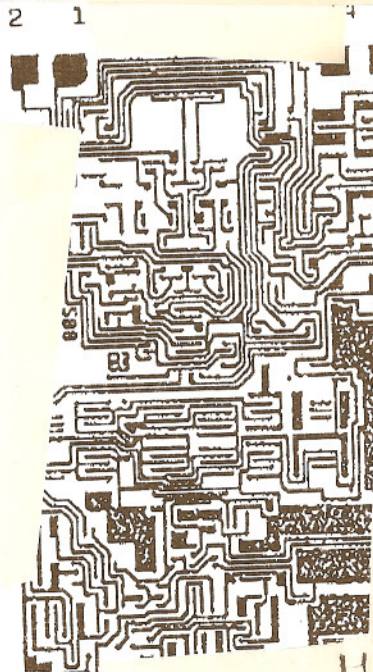
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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

1	IN-
2	IN+
3	OFFSET ADJL
4	OFFSET ADJR
5	V-
6	NC
7	OUTPUT
8	NC
9	V+
10	NC
11	HOLD CAPACITOR
12	NC
13	GND
14	S/H CONTROL



14 MUST BE CONNECTED TO -V

Topside Metal: Al

Backside: Si

Backside Potential:

Mask Ref:

Bond Pads : .004" Min

APPROVED BY: CB

MFG: Harris

DIE SIZE : .061" x .097"

THICKNESS: .020"

DATE: 1/25/01

P/N: HA0-2420-2