

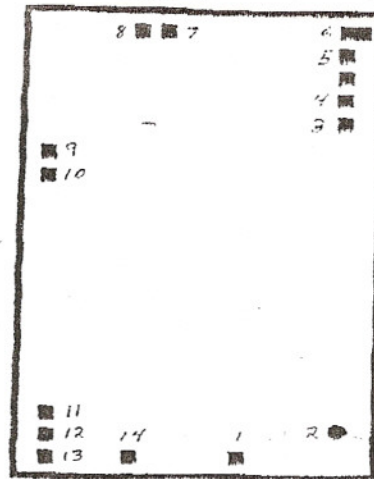


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



1. Mfr. Supertex Inc.
2. Die size: .065 X .105 ± .003
3. Metallization: Topside - Al; Backside - Au or Si

FIGURE 2 - DIE CONFIGURATION

Topside Metal: Al

Backside: Si

Backside Potential:

Mask Ref:

Bond Pads : .004 min

APPROVED BY: CB

MFG: Supertex

DIE SIZE: .065" x .105"

THICKNESS: .019"

DATE: 2/6/01

P/N: HV9110X