Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**.129”**

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[**https://www.fedex.com/fedextracking/**](https://www.fedex.com/fedextracking/) **Fedex Tracks**

[**https://www.staplesadvantage.com/sahome?fromWhere=rmbrMe&from=httpdconf-sm&routeType=sba&billTo=b64BillTo&shipTo=b64ShipTo&onLoad=hideMessage**](https://www.staplesadvantage.com/sahome?fromWhere=rmbrMe&from=httpdconf-sm&routeType=sba&billTo=b64BillTo&shipTo=b64ShipTo&onLoad=hideMessage) **staples**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .087” X .087” DATE: 4/20/23**

**MFG: SILICON SUPPLIES THICKNESS .000” P/N: 1N5417**

**DG 10.1.2**

#### Rev B, 7/1